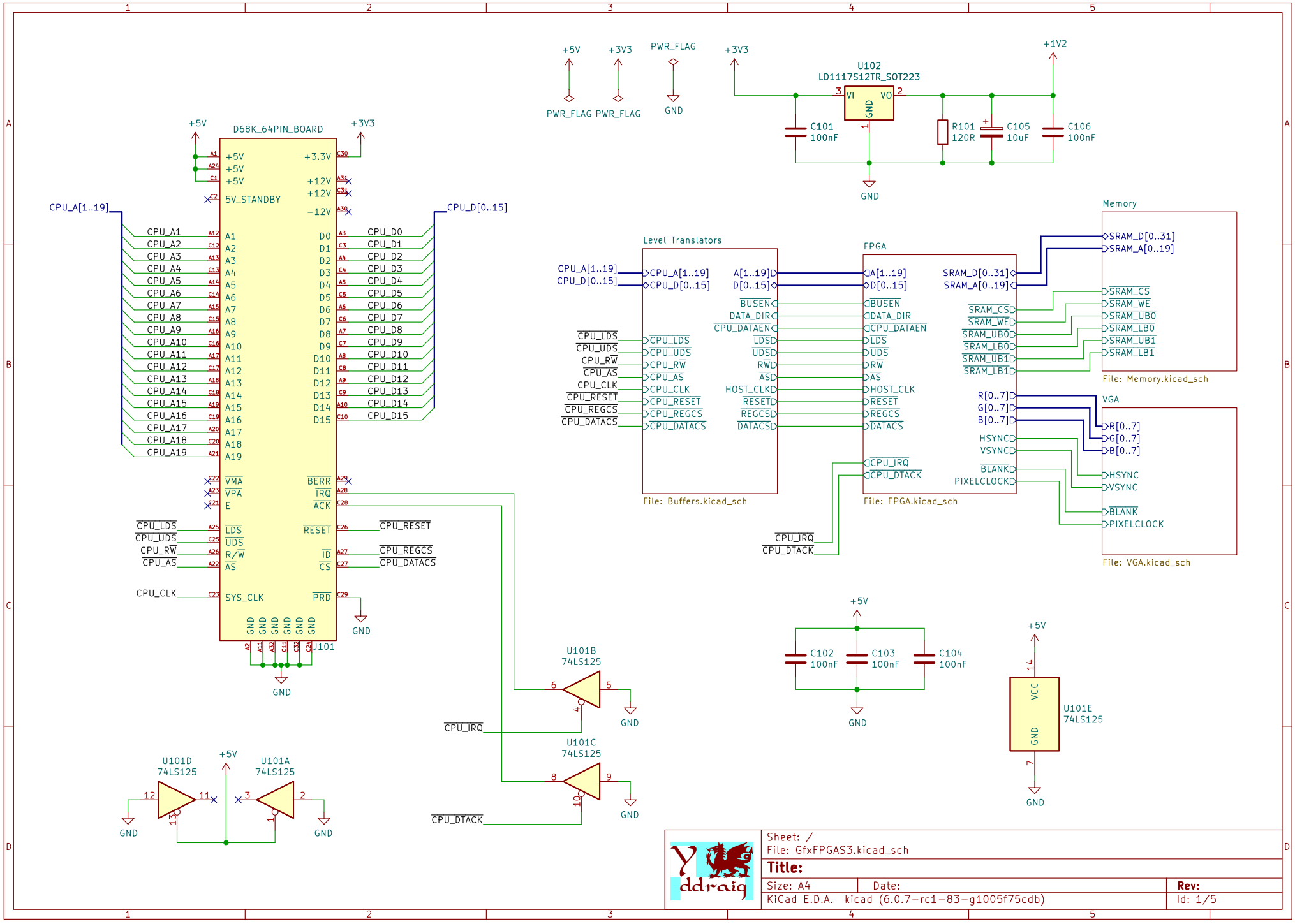
+5V
+3V3
PWR_FLAG
PWR_FLAG PWR_FLAG
GND
+3V3
U102
LD1117S12TR_SOT223
VI
VO
GND
+1V2
C101
100nF
R101
120R
C105
10uF
C106
100nF
GND
D68K_64PIN_BOARD
+5V
+3V3
5V_STANDBY
+3.3V
+12V
-12V
CPU_A[1..19]
CPU_D[0..15]
CPU_A1
CPU_A2
CPU_A3
CPU_A4
CPU_A5
CPU_A6
CPU_A7
CPU_A8
CPU_A9
CPU_A10
CPU_A11
CPU_A12
CPU_A13
CPU_A14
CPU_A15
CPU_A16
CPU_A17
CPU_A18
CPU_A19
CPU_D0
CPU_D1
CPU_D2
CPU_D3
CPU_D4
CPU_D5
CPU_D6
CPU_D7
CPU_D8
CPU_D9
CPU_D10
CPU_D11
CPU_D12
CPU_D13
CPU_D14
CPU_D15
VMA
VPA
E
BERR
IRQ
ACK
CPU_LDS
CPU_UDS
CPU_RW
CPU_AS
LDS
UDS
R/W
AS
RESET
ID
CS
CPU_RESET
CPU_REGCS
CPU_DATACS
CPU_CLK
SYS_CLK
PRD
GND
J101
Level Translators
CPU_A[1..19]
CPU_D[0..15]
CPU_LDS
CPU_UDS
CPU_RW
CPU_AS
CPU_CLK
CPU_RESET
CPU_REGCS
CPU_DATACS
A[1..19]
D[0..15]
BUSEN
DATA_DIR
CPU_DATAEN
LDS
UDS
RW
AS
HOST_CLK
RESET
REGCS
DATACS
File: Buffers.kicad_sch
FPGA
CPU_IRQ
CPU_DTACK
SRAM_D[0..31]
SRAM_A[0..19]
SRAM_CS
SRAM_WE
SRAM_UB0
SRAM_LB0
SRAM_UB1
SRAM_LB1
R[0..7]
G[0..7]
B[0..7]
HSYNC
VSYNC
BLANK
PIXELCLOCK
File: FPGA.kicad_sch
Memory
File: Memory.kicad_sch
VGA
File: VGA.kicad_sch
U101B
74LS125
U101C
74LS125
U101D
74LS125
U101A
74LS125
U101E
74LS125
VCC
C102
100nF
C103
100nF
C104
100nF
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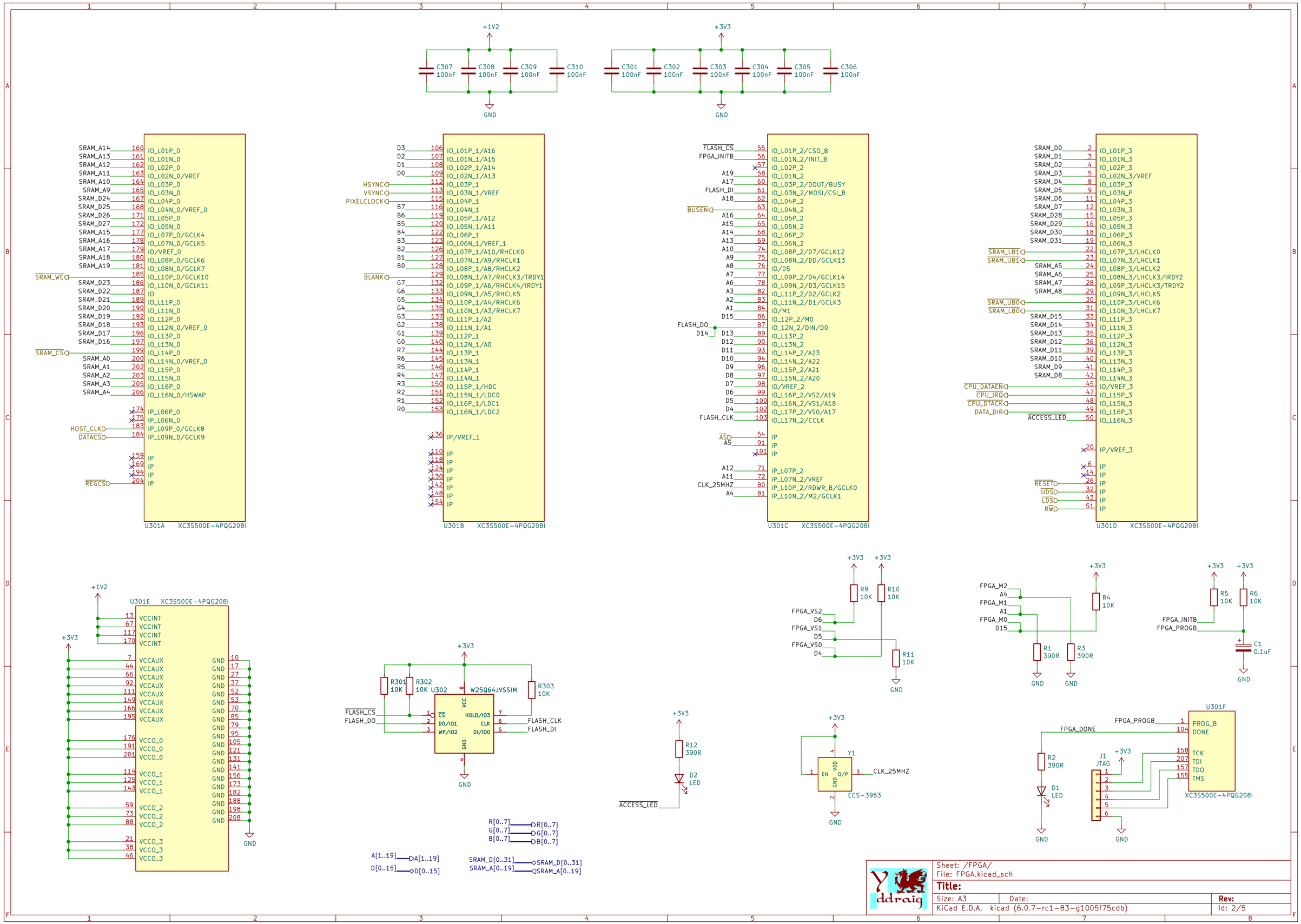
Date:
Rev:
KiCad E.D.A. kicad (6.0.7-rc1-83-g1005f75cdb)
Id: 1/5


+1V2
C307 100nF
C308 100nF
C309 100nF
C310 100nF
GND
+3V3
C301 100nF
C302 100nF
C303 100nF
C304 100nF
C305 100nF
C306 100nF
GND
U301A XC3S500E-4PQG208I
U301B XC3S500E-4PQG208I
U301C XC3S500E-4PQG208I
U301D XC3S500E-4PQG208I
U301E XC3S500E-4PQG208I
U301F
XC3S500E-4PQG208I
U302 W25Q64JVSSIM
R301 10K
R302 10K
R303 10K
R9 10K
R10 10K
R11 10K
R4 10K
R1 390R
R3 390R
R5 10K
R6 10K
C1 0.1uF
R2 390R
D1 LED
J1 JTAG
R12 390R
D2 LED
Y1 ECS-3963
FLASH_CS
FLASH_DO
FLASH_CLK
FLASH_DI
ACCESS_LED
CLK_25MHZ
FPGA_PROGB
FPGA_DONE
R[0..7]
G[0..7]
B[0..7]
A[1..19]
D[0..15]
SRAM_D[0..31]
SRAM_A[0..19]
Sheet: /FPGA/
File: FPGA.kicad_sch
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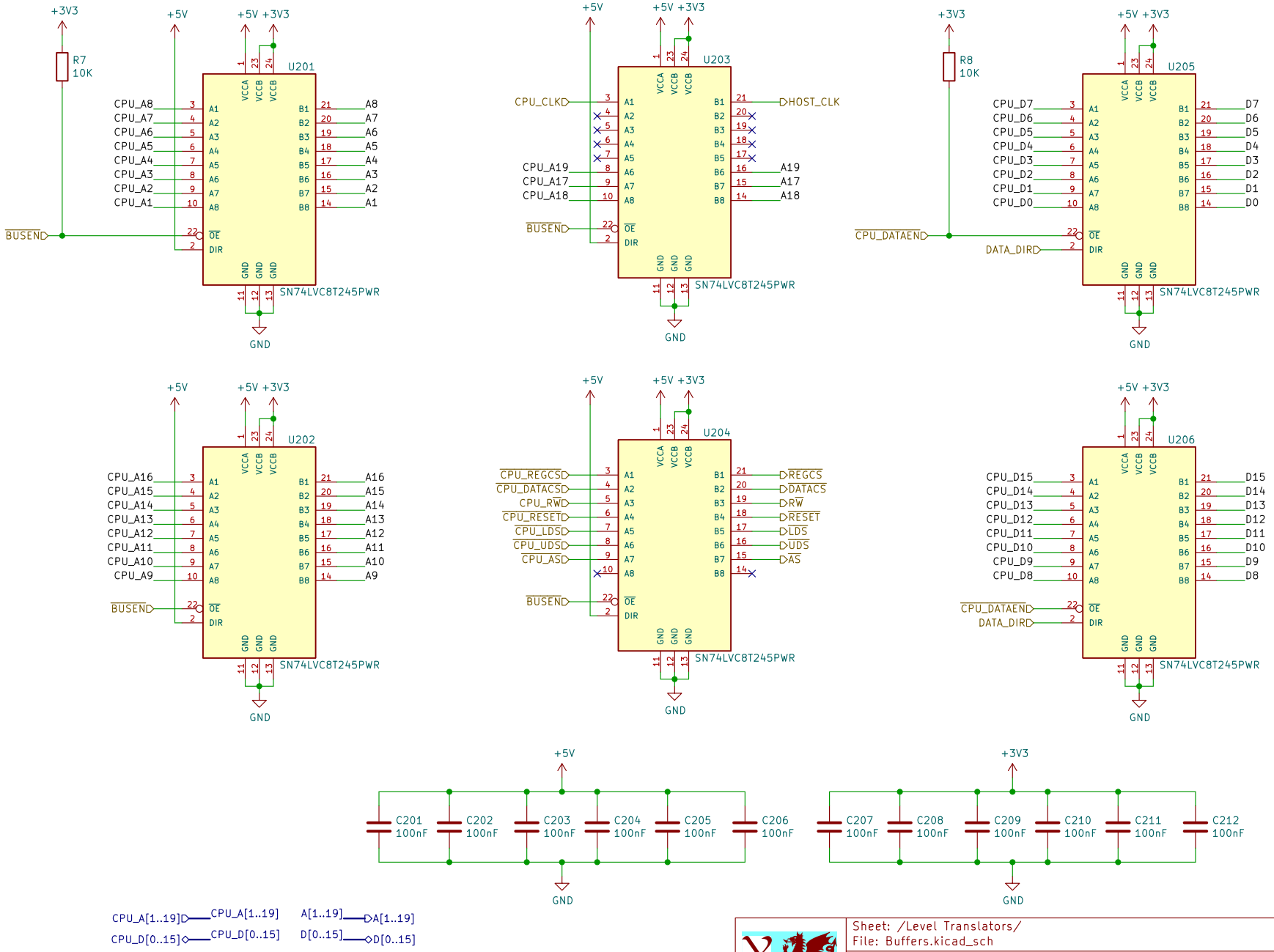
Date:
Rev:
KiCad E.D.A. kicad (6.0.7-rc1-83-g1005f75cdb)
Id: 2/5




Sheet: /Level Translators/
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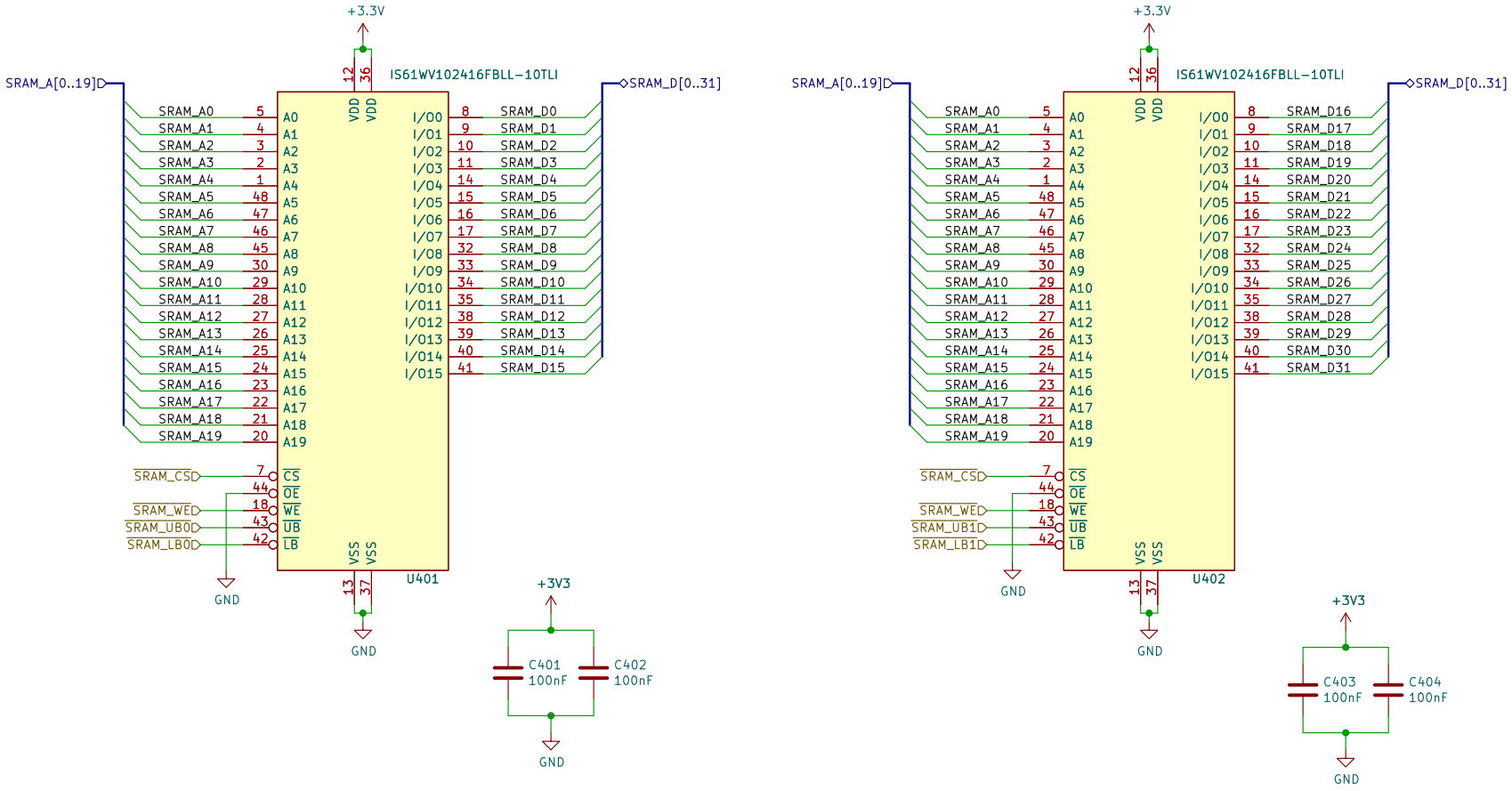
| KiCad E.D.A. kicad (6.0.7-rc1-83-g1005f75cdb) | | Id: 3/5 |

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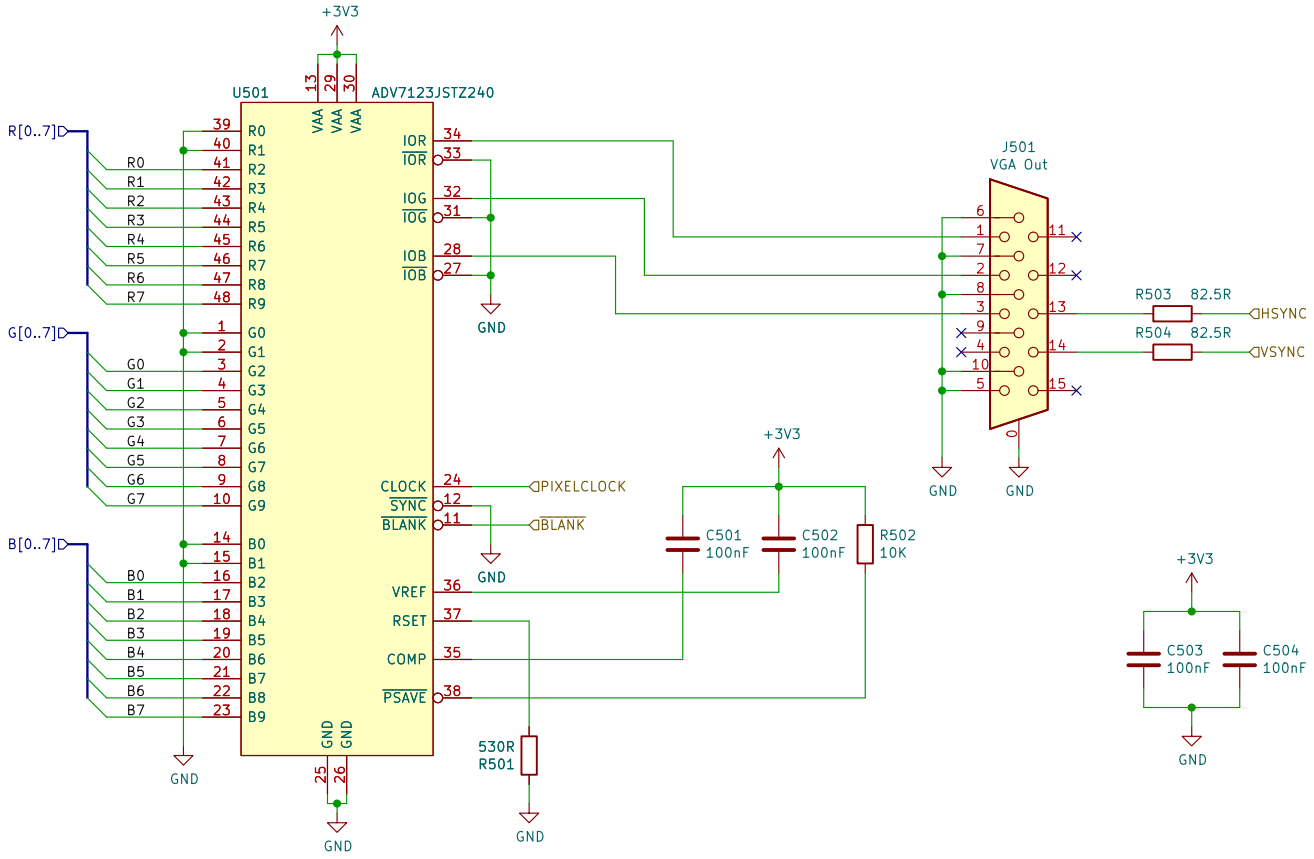


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